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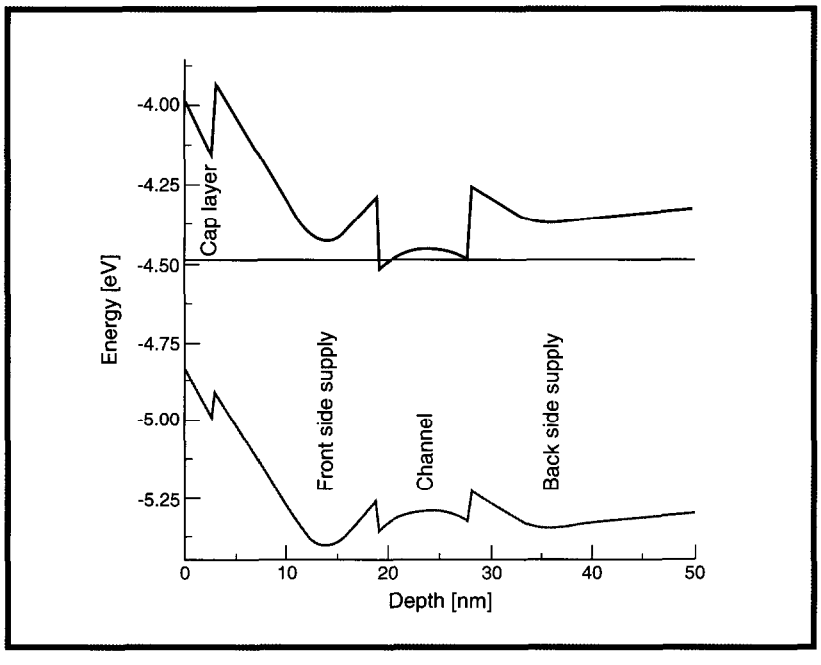
The use of the silicon-based High Electron Mobility Transistor (HEMT) for coming generations of high-frequency electronics is favoured by the need for reduced cost. Furthermore, the combination of different growth technologies like LEPECVD and MBE enables the realization of SiGe device structures with excellent performance.

HEMTs on LEPECVD-grown virtual SiGe substrates

Analogue high-frequency electronics in the range between 1 GHz (wireless communication) and 100 GHz (radar) are still dominated by GaAs-based devices like HEMTs and HBTs. However, forced by cost restrictions, especially in the cell-phone market, in recent years SiGe HBTs have emerged as a lower-cost alternative (though SiGe HEMTs are still at the research status).

Unlike AlGaAs-on-GaAs, SiGe-on-silicon is a highly lattice-mismatched material system. However, although it suffers from defect generation during growth, it offers the possibility of strain engineering.

Figure 1. Graph of energy-depth profile for an n-type SiGe/Si HEMT. Carrier confinement results from the formation of a type-II heterostructure band offsets in the Si/SiGe material system due to the in-plane tensile strain in a silicon layer on a virtual substrate (VS) with a larger lattice constant - i.e. relaxed SiGe on Si(100).



A key element for the realization of a strained silicon channel with high electron mobility is the so-called virtual substrate which is produced by epitaxial deposition of a strain-relieved SiGe alloy layer on a standard silicon wafer.

Currently, the preparation of a high-quality virtual substrate with low defect density requires a very thick (several µm) epitaxial layer. For sufficient process throughput a high growth rate is essential. This is in sharp contrast to the requirements for the deposition of active HEMT layers (i.e. low growth rate) to get interface abruptness and precise thickness control on a nanometre scale. The problem of these widely spaced process parameters can be overcome through a combination of growth technologies like MBE and low-energy plasma-enhanced chemical vapour deposition (LEPECVD).

SiGe HEMT basics

Unlike GaAs-based HEMTs, strain is an indispensable prerequisite to achieve a band offset for carrier confinement in the Si/SiGe material system. N-type HEMTs require an in-plane tensile-strained Si layer on a virtual substrate (VS) with a larger lattice constant than Si - i.e. relaxed SiGe on Si(100) - to create a quantum well (QW) for electrons. Due to the tensile strain in

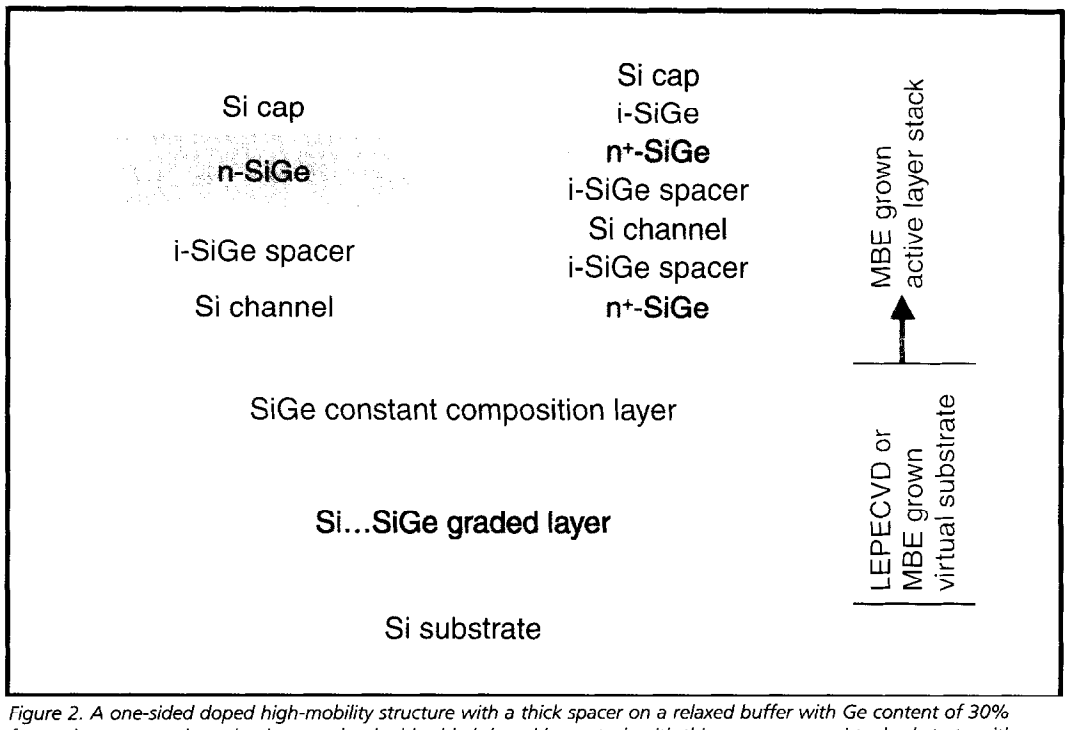


Figure 2. A one-sided doped high-mobility structure with a thick spacer on a relaxed buffer with Ge content of 30% for carrier transport investigations; and a double-sided doped layer stack with thin spacers on a virtual substrate with a composition of 40% for device preparation.

the silicon, a type-II heterostructure is formed (see Figure 1).

For high-frequency applications, the combination of silicon QWs and $Si_{0.55}Ge_{0.45}$ buffers has proven to be a good compromise between high sheet carrier concentration and acceptable mobility. Growth procedure and surface morphology (cross-hatch) are very similar to so-called metamorphic InGaAs devices on GaAs substrates.

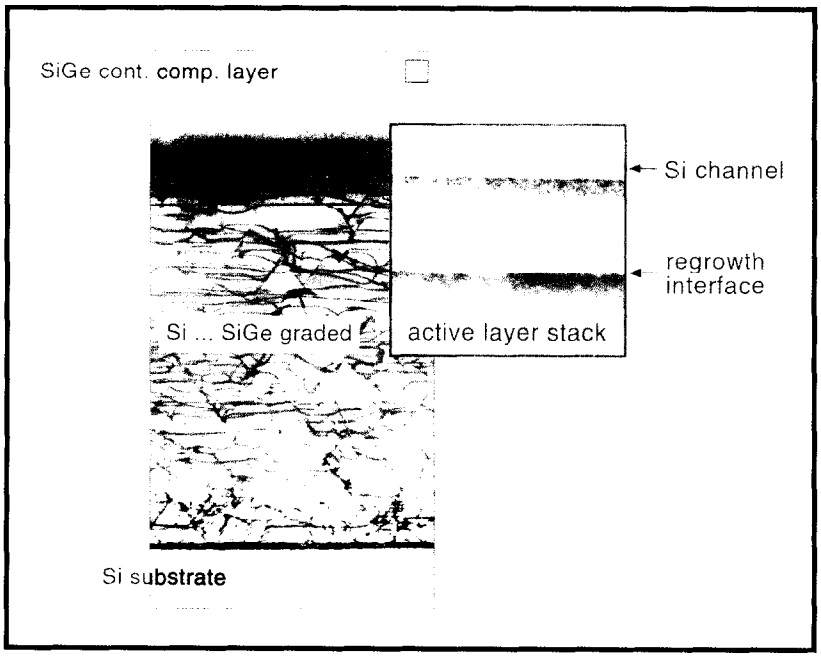
The relaxation of the strain in SiGe-on-Si substrates is accomplished by the formation of misfit dislocations parallel to the interface. As a detrimental side-effect, additional threading dislocations occur which pierce the transistor channel and deteriorate the mobility of the carriers. Until now, virtual substrates with lowest threading dislocation density have been achieved by growing thick SiGe layers with a shallow composition grading. Doing this with MBE ends up with unreasonably long growth times (several hours) and an unacceptably high consumption of source material (10-20% of the source charge).

Mixed technology approach

The low-energy plasma-enhanced CVD (LEPECVD) experimental system (4") is based on a Unaxis UHV reactor originally developed for dry cleaning of semiconductor surfaces. The low discharge voltage (< 25 V) and high electron current (up to 70 A) enable efficient cracking of the source gases (silane and germane) without generating ion defects. Focusing the plasma onto the wafer results in a high surface energy and enables extremely large growth rates - up to 20 times higher than MBE [1].

At the Solid State Physics Laboratory of ETH Zürich/Switzerland relaxed buffers with a SiGe

Figure 3. TEM cross section showing typical defect structure for relaxed buffers, with a high density of misfit and threading dislocations in the compositionally graded region and a defect-free constant-composition region above it.



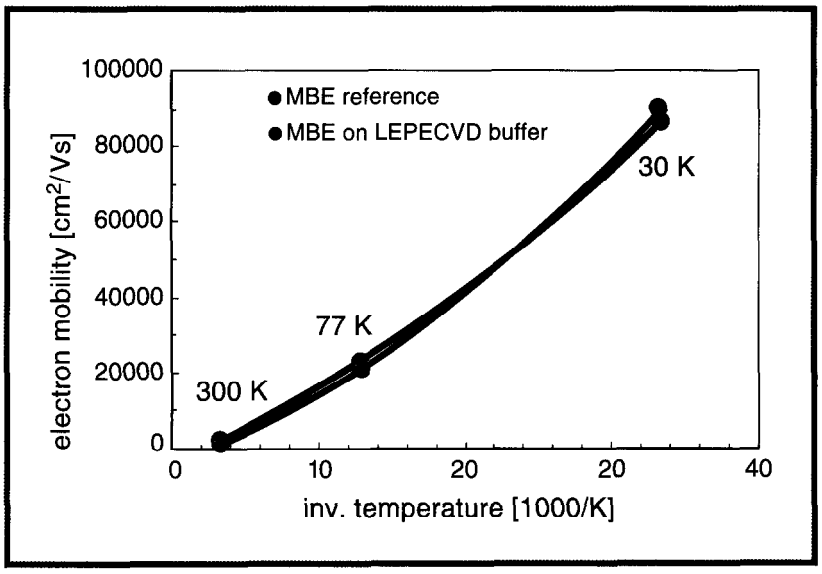
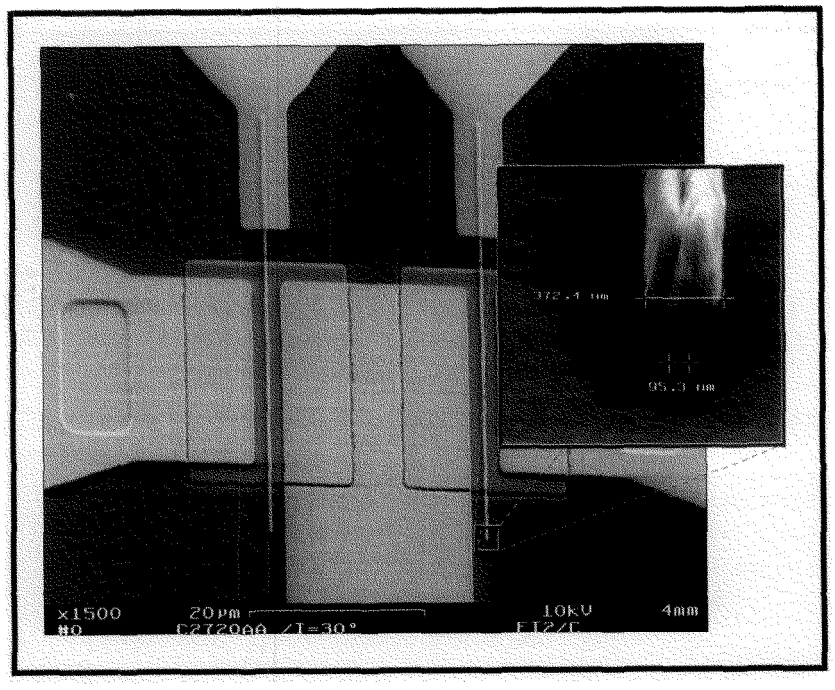


Figure 4. At 30 K the mixed technology sample shows an outstanding mobility of more than 88,000 cm²/Vs compared to 86,000 cm²/Vs for the reference structure.

composition grading of 10%/μm and a 1 μm thick constant composition layer were prepared by LEPECVD. These virtual substrates were overgrown with n-type SiGe HEMT structures at the DaimlerChrysler Research Center in Ulm, Germany by MBE (using a Balzers UMS 630 system). Two versions were realized (see Figure 2):

- a one-sided doped high-mobility structure with a thick spacer on a relaxed buffer with Ge content of 30% for carrier transport investigations; and
- a double-sided doped layer stack with thin spacers on a virtual substrate with a composition of 40% for device preparation.

Figure 5. For high-frequency applications, transistor devices were produced at DaimlerChrysler AG using a T-shaped gate with a footprint of about 100 nm.



For comparison, reference structures were grown entirely by MBE but with a gradient of 20%/μm and a constant composition layer only 0.5 μm thick (to reduce growth time and material consumption).

Results

Transmission electron microscopy in cross section shows the typical defect structure for these types of relaxed buffers, with a high density of misfit and threading dislocations in the compositionally graded region and a defect-free constant-composition region above it (see Figure 3). Even the LEPECVD/MBE re-growth interface appears free of crystal defects.

This excellent structural quality results in a very high room-temperature electron mobility, exceeding 2000 cm²/Vs at a sheet carrier concentration of 10^{12} cm^{-2} for both versions. At 30 K the mixed technology sample shows an outstanding mobility of more than 88,000 cm²/Vs compared to 86,000 cm²/Vs for the reference structure (see Figure 4). This is probably due to a lower defect density in this type of large-thickness buffer.

For high-frequency applications, transistor devices were produced at DaimlerChrysler AG using a T-shaped gate with a footprint of about 100 nm (see Figure 5) [2]. Comparing the figures of merit of both technologies shows 10-20% better device results for the mixed technology in all cases (see Figure 6). This more surprising because in this case the wafers were subject to storage in ambient atmosphere, transportation and additional wet cleaning before regrowth.

Outlook

Even better results can be expected by combining LEPECVD with a low-rate growth system like MBE or UHVCVD in a cluster tool, thereby enabling wafer transfer under UHV conditions between buffer and active layer preparation.

In this configuration, the processing time per HEMT structure growth (including *in situ* surface conditioning etc) could be reduced to 60 minutes compared to 180 minutes necessary for entire MBE growth.

Moreover, the quantity of wafers prepared with one source charge of the MBE system

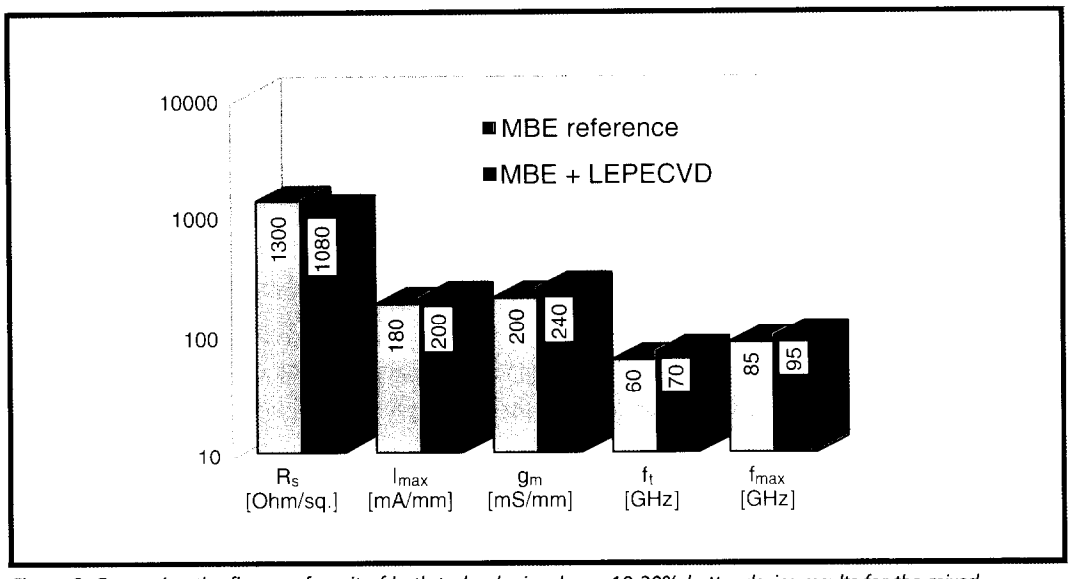


Figure 6. Comparing the figures of merit of both technologies shows 10-20% better device results for the mixed technology in all cases.

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can be enhanced by a factor of 40, enabling a tremendous reduction in epitaxy costs. Shorter running time and less down time result in a potential enhancement in throughput by about a factor of four (single-shift operation) to eight (double-shift operation).

Another approach is the complete processing of HEMT structures by LEPECVD. Unaxis Semiconductors has developed a 300 mm single-wafer cluster tool which combines in-situ low-temperature pre-epi clean with the LEPECVD process (see Figure 7). Based on this, complete dry processing for virtual substrates and possibly also for HEMT structures can be envisaged.

References

[1] C Rosenblad *et al, Appl. Phys. Lett.* **76** (2000) 427

[2] M Zeuner *et al, IEEE Microwave and Guided Wave Letters* **9** (1999) 410

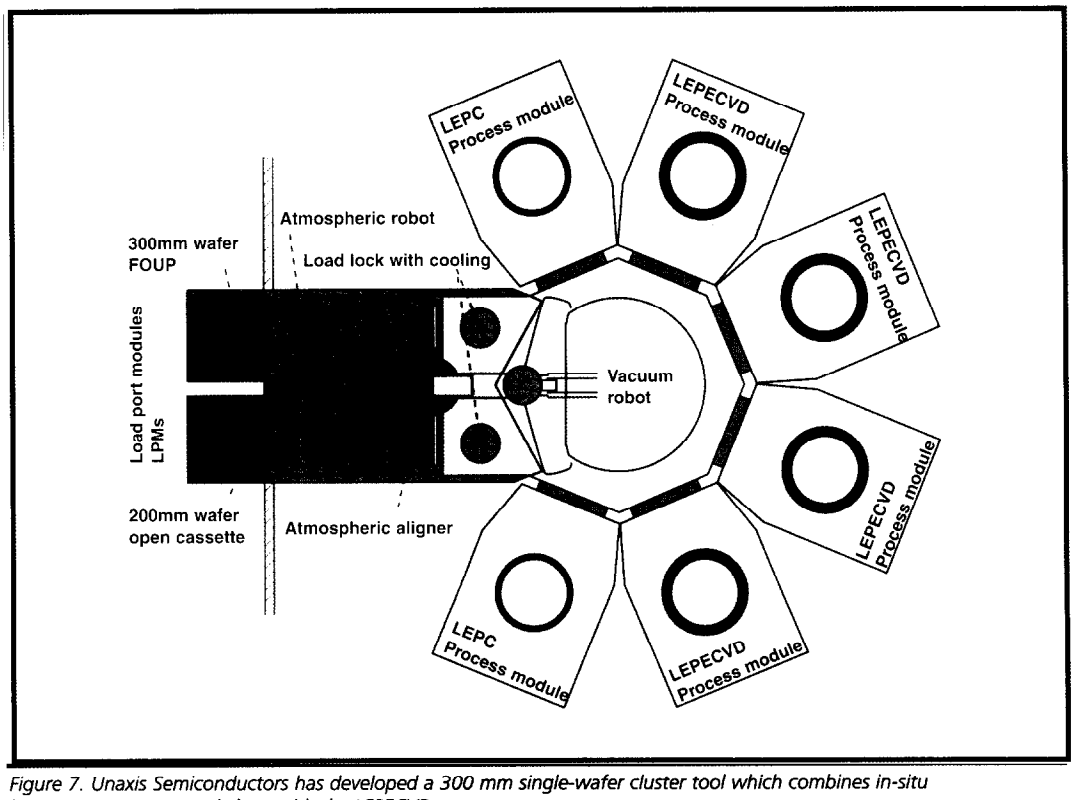

Figure 7. Unaxis Semiconductors has developed a 300 mm single-wafer cluster tool which combines in-situ low-temperature pre-epi clean with the LEPECVD process.